Space Radiation Effects On Low Power Advanced-Technology DRAMs

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Abstract

Space radiation effects on highly scaled low power memories have been investigated. Scaling and voltage reduction generally reduce the radiation tolerance of microelectronic components. Two distinct ionizing radiation degradation mechanisms contributing to component failure are presented. Also discussed are heavy ion data taken from highly scaled DRAMs that show new hard error effects that are expected to become worse as devices are scaled further.

Space Radiation Effects on VLSI Devices

Integrated circuits are continuing to advance rapidly. Several manufacturers have 1Gb DRAMs in development [1,?] and there have been several recent studies on alternative CMOS scaling approaches for low power circuits [3,4]. This continued advancement in scaling and circuit density also impacts the performance of advanced devices in space which are required to operate after exposure levels of 20-100 krad(Si).

Effects of scaling on the ability of CMOS integrated circuits to withstand ionizing radiation have been investigated for some time. [5-8]. For example, when gate oxides are thinned, there is a general reduction in radiation-induced threshold voltage shift. This threshold voltage shift generally follows a t_{OX}^2 relationship [5, 8]. The benefit of thinning gate oxides is clear, but these gains can be offset by changes in circuit design and internal operating margins which are necessary to circuits designed with highly scaled devices.

Even though the gate oxide is thinned, field oxides are still relatively thick (100's of nm) and field oxide inversion is often the dominate mechanism for total ionizing dose (TID) failure.. Reducing the operating voltage of CMOS circuits below 5 volts can have beneficial effects, but there are inevitable trade-offs in circuit operational and radiation performance. Reduction in noise margins as scaling increases may result in early total dose failure in highly scaled devices.

As device geometries are scaled down, device dimensions are scaled by differing factors. Polysilicon and silicon oxide layers must be thinned to maintain performance [9]. As MOS transistor gate lengths are reduced to below 0.8 pm, the supply voltage must be reduced to avoid hot carrier reliability issues. The rapid advance in DRAM density makes this technology a good choice as a test vehicle for studying the effects of increased density and reduction in supply voltage on the radiation response of highly scaled devices.

New Results for Low-Voltage and Scaled Devices

Figure 1 shows standby supply current as a function of dose for several high density DRAMs including a 64Mb 3.3V fast page mode DRAM. Two classes of behavior can be seen. The rapid degradation

The work described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration under the NASA Code Q Microelectronics Space Radiation Effects Program (MSREP).

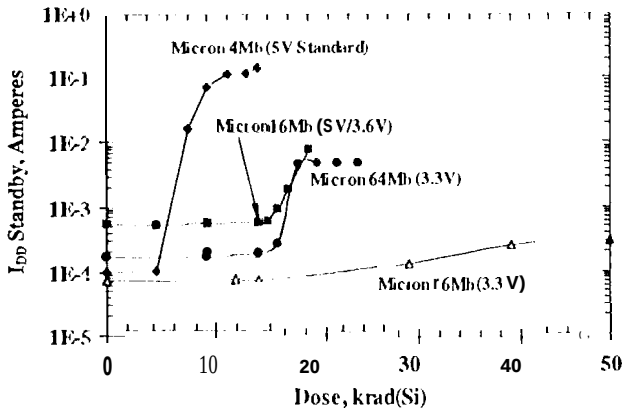

Figure 1. I_{DD} standby vs. ionizing dose for several DRAMs including a 64Mb fast page mode 3.3V DRAM. Note the large increase in supply current at 5 and 15 krad(Si) vs the gradual degradation exhibited by the 3.3V 16Mb DRAM.

of current exhibited by three of the devices in Figure 1 (curves with large increases at 5 and 15 krad(Si)) can be explained by trapped charge in the field oxide where huge parasitic leakage paths can be developed. Another class of ionizing radiation degradation is seen where supply current gradually increases with radiation and it is characterized by the fourth curve in Figure 1. In these cases, device failure may occur due to gate oxide ionization damage. which shifts the subthreshold characteristics of the DRAM memory cell access transistors. An example of the subthreshold curves after various radiation doses for an n-FET from a 3.6V DRAM process is shown in Figure 2. Note. that V_t shifts negatively and eventually develops large-parasitic leakage paths at the eight.it dose of 55 krad(Si).

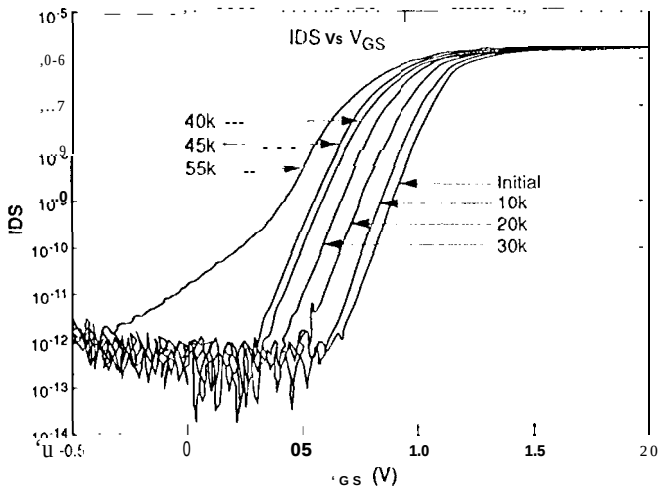

Figure 2. Subthreshold Characteristics for a 3.6V DRAM cell access transistor. Note the large parasitic leakage that has developed at 55 krad(Si)

The change in subthreshold leakage also causes retention time to decrease with radiat ion. 1 'igure 3 shows retention ti nc data for the 10% of the bits with the shortest retention times for two 16Mb I DRAMs. Mean retention time decreases significantly with increasing levels of radiation, but first bit retention ti mes are less affected. The distribution of retention times is determined by a number of factors including statistical variations in the threshold voltage and operating margins of the individual cells. The times were. measured at 40°C and would be much shorter at higher temperatures

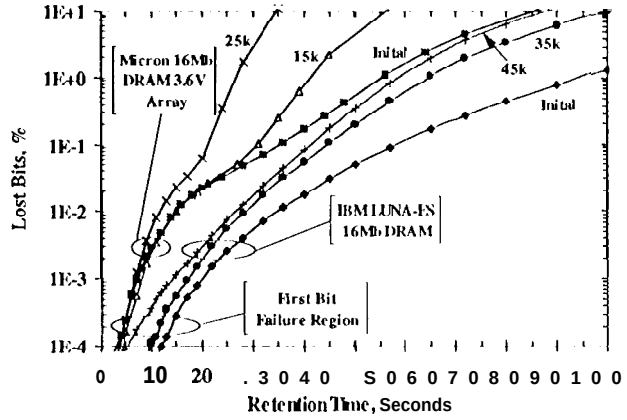

Figure 3. Percentage of bit failure vs. retention time for two 16Mb DRAMs Note that much larger shifts occur at higher percentages than at low percentages.

Heavy Ion Effects in High-Density Low Voltage DRAMs

A heavy ion (from alpha particles on up) strike creates a dense track of electrons and holes; thus the net effect of radiation damage from heavy ions increases as feature-size is reduced to the point that it is comparable in size to the diameter of the ion track. Three main categories of single ion-induced (or "single event") effects are (1) the upset of storage elements, (2) dielectric breakdown, and (3) localized dose damage or "microdose."

When device dimensions are reduced to the point where the area of the microdose created by a single particle is comparable to the active gate region, it is possible for the localized damage from a single interaction to affect an individual MOS transistor. Such effects were unimportant for devices with feature. sizes above 1.0μm because several heavy ions would have to strike the gate region in order to cause sufficient damage, which has low statistical probability. The localized residual in dose damage lasts for some time, but may partially anneal with time and/or elevated temperature. Microdose damage has been definitively observed [10,11] in devices with feature sizes < 0.8 μm, demonstrating that feature sizes are now small enough for microdose to be a significant and increasing problem.

Retention time is a useful tool in the study of microdose effects in DRAMs. Figure 4 shows retention time distributions for two 4Mb DRAMs with two different feature sizes from the same manufacturer. Ions with moderately dense ionization tracks cause a distribution of retention time reductions base.(i on the statistical nature of tile nearness of the strike to sensitive gate regions and the charge trapping process. Note that the smaller feature size de.vice is more. affected, as expected. As feature. size is further reduced, the deposited microdose from a given ion species and energy increase.s and the number of ions capable of a given dose increase.s rapidly

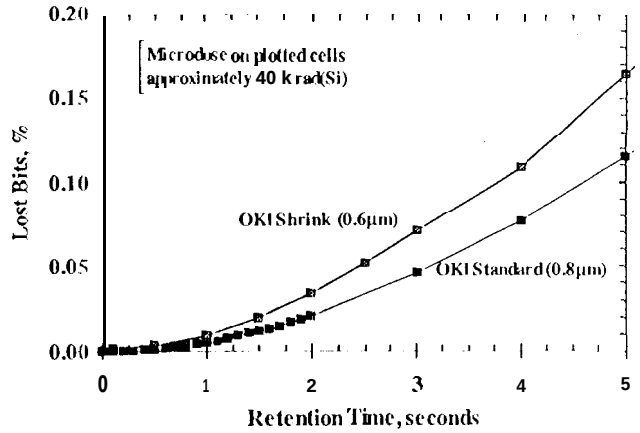

Figure 4. Retention time data after heavy ioa irradiation showing the microdose effect on DRAMs with two feature sizes from the same manufacturer.

Future Trends

Although some improve. nent in total dose hardness is expected from reduction in gate oxide thickness, test results show that scaling dots not consistently improve radiation response for conventional total dose environments. The underlying reasons are field oxide inversion, because field oxides do not scale with other device dimensions, and internal operating margins, which are lower for highly scaled devices. For single event effects, one can expect reduced device performance due to transistor subthreshold leakage (microdose) and ion-induced gale rupture. Experimental data show that as device size approaches heavy ion track diameters, single ion strikes are more capable of seriously disrupting memory cell performance in space applications, The microdose problem will become more severe as devices are scaled further, and will become important for other types of VLSI devices as well as memories.

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